Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **CLEAR**
2. **1Q**
3. **N. 1Q**
4. **1D**
5. **2D**
6. **N. 2Q**
7. **2Q**
8. **GND**
9. **CLOCK**
10. **3Q**
11. **N. 3Q**
12. **3D**
13. **4D**
14. **N. 4Q**
15. **4Q**
16. **VCC**

**14 13 12 11**

**3 4 5 6**

**15**

**16**

**1**

**2**

**10**

**9**

**8**

**7**

**L S**

**1 7**

**5 A**

**MASK**

**REF**

**.050”**

**.060”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: LS175A**

**APPROVED BY: DK DIE SIZE .050” X .060” DATE: 8/29/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: 54LS175**

**DG 10.1.2**

#### Rev B, 7/1